Exercice 2 : écrire ce qui se passe lors des étapes de l’exécution de l’instruction suivante : M = T1 \* T2

Cette instruction est placée en RAM à l’adresse 2A96.

Les variables T1,T2 et M prennent chacun 1 octet signé et sont placées en RAM respectivement aux adresses 2B01, 2B02 et 2B03.

Les valeurs lues pour T1 et T2 sont respectivement : 410 et -1210

Commencer à partir de l’étape 2, une fois que l’instruction est dans le CPU.

Faire des copies du gabarit de la page suivante tant que nécessaire…

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| |  |  |  | | --- | --- | --- | |  | Registres  (8 bits) |  | |  | M = T1 \* T2 |  | |  | 00000100 | UAL | |  | 11110100 | |  | | --- | |  | | |  |  | |  |  | |  |  |  |  |  |  |  | | --- | --- | --- | |  |  |  | |  | Unité de contrôle |  | |  | |  |  | | --- | --- | |  |  | | **Adresses**  **16 bits** | **Contenu**  **8 bits** | |  | … | | 2A96 | M = T1 \* T2 | |  |  | | 2B01 | 00000100 | | 2B02 | 11110100 | | 2B03 |  | |  |  |   L’unité de contrôle demande à l’UAL de faire l’opération arithmétique : (4\*-12) = -48 | variables |
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| |  |  |  | | --- | --- | --- | |  | Registres  (8 bits) |  | |  | M = T1 \* T2 |  | |  | 00000100 | UAL | |  | 11110100 | |  | | --- | |  | | |  | 11010000 | |  |  | |  |  |  |  |  |  |  | | --- | --- | --- | |  |  |  | |  | Unité de contrôle |  | |  | |  |  | | --- | --- | |  |  | | **Adresses**  **16 bits** | **Contenu**  **8 bits** | |  | … | | 2A96 | M = T1 \* T2 | |  |  | | 2B01 | 00000100 | | 2B02 | 11110100 | | 2B03 |  | |  |  | | variables |
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| |  |  |  | | --- | --- | --- | |  | Registres  (8 bits) |  | |  | M = T1 \* T2 |  | |  | 00000100 | UAL | |  | 11110100 | |  | | --- | |  | | |  | 11010000 | |  |  | |  |  |  |  |  |  |  | | --- | --- | --- | |  |  |  | |  | Unité de contrôle |  | |  | |  |  | | --- | --- | |  |  | | **Adresses**  **16 bits** | **Contenu**  **8 bits** | |  | … | | 2A96 | M = T1 \* T2 | |  |  | | 2B01 | 00000100 | | 2B02 | 11110100 | | 2B03 | 11010000 | |  |  | | variables |
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**Solution**

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| |  |  |  | | --- | --- | --- | |  | Registres  (8 bits) |  | |  | M = T1\*T2 |  | |  |  | UAL | |  |  | |  | | --- | |  | | |  |  | |  |  | |  |  |  |  |  |  |  | | --- | --- | --- | |  |  |  | |  | Unité de contrôle |  | | Transférer ds le CPU 🡪 | |  |  | | --- | --- | |  |  | | **Adresses**  **16 bits** | **Contenu**  **8 bits** | |  | … | | 2A96 | M = T1\*T2 | |  | … | | 2B01 | 00000100 | | 2B02 | 11110100 | | 2B03 |  | |  |  |   Étape 1 : L’unité de contrôle demande à la RAM de lui envoyer le contenu de l’adresse 2B01 (bus de contrôle (orange) et bus d’adresses (vert)) | variables |
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| |  |  |  | | --- | --- | --- | |  | Registres  (8 bits) |  | |  | M = T1\*T2 |  | |  | 00000100 | UAL | |  |  | |  | | --- | |  | | |  |  | |  |  | |  |  |  |  |  |  |  | | --- | --- | --- | |  |  |  | |  | Unité de contrôle |  | | Transférer ds le CPU 🡪 | |  |  | | --- | --- | |  |  | | **Adresses**  **16 bits** | **Contenu**  **8 bits** | |  | … | | 2A96 | M = T1\*T2 | |  | … | | 2B01 | 00000100 | | 2B02 | 11110100 | | 2B03 |  | |  |  |   Étape 3 : L’unité de contrôle demande à la RAM de lui envoyer le contenu de l’adresse 2B02 (bus de contrôle (orange) et bus d’adresses (vert)) | variables |
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| |  |  |  | | --- | --- | --- | |  | Registres  (8 bits) |  | |  | M = T1\*T2 |  | |  | 00000100 | UAL | |  |  | |  | | --- | |  | | |  |  | |  |  | |  |  |  |  |  |  |  | | --- | --- | --- | |  |  |  | |  | Unité de contrôle |  | |  | |  |  | | --- | --- | |  |  | | **Adresses**  **16 bits** | **Contenu**  **8 bits** | |  | … | | 2A96 | M = T1\*T2 | |  | … | | 2B01 | 00000100 | | 2B02 | 11110100 | | 2B03 |  | |  |  |   Étape 4 : La RAM envoie la valeur demandée via le bus de données (bleu) | variables |
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| |  |  |  | | --- | --- | --- | |  | Registres  (8 bits) |  | |  | M = T1\*T2 |  | |  | 00000100 | UAL | |  | 11110100 | |  | | --- | |  | | |  |  | |  |  | |  |  |  |  |  |  |  | | --- | --- | --- | |  |  |  | |  | Unité de contrôle |  | |  | |  |  | | --- | --- | |  |  | | **Adresses**  **16 bits** | **Contenu**  **8 bits** | |  | … | | 2A96 | M = T1\*T2 | |  | … | | 2B01 | 00000100 | | 2B02 | 11110100 | | 2B03 |  | |  |  |   Étape 5 : L’unité de contrôle demande à l’UAL de faire l’opération arithmétique (4\* -12)  Résultat : -48 = 11010000 en représentation interne | variables |
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| |  |  |  | | --- | --- | --- | |  | Registres  (8 bits) |  | |  | M = T1\*T2 |  | |  | 00000100 | UAL | |  | 11110100 | |  | | --- | |  | | |  | 11010000 | |  |  | |  |  |  |  |  |  |  | | --- | --- | --- | |  |  |  | |  | Unité de contrôle |  | |  | |  |  | | --- | --- | |  |  | | **Adresses**  **16 bits** | **Contenu**  **8 bits** | |  | … | | 2A96 | M = T1\*T2 | |  | … | | 2B01 | 00000100 | | 2B02 | 11110100 | | 2B03 |  | |  |  |   Étape 6 : Le résultat de l’opération arithmétique (1101000) est placé dans un registre du CPU | variables |
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| |  |  |  | | --- | --- | --- | |  | Registres  (8 bits) |  | |  | M = T1\*T2 |  | |  | 00000100 | UAL | |  | 11110100 | |  | | --- | |  | | |  | 1101000 | |  |  | |  |  |  |  |  |  |  | | --- | --- | --- | |  |  |  | |  | Unité de contrôle |  | | Transférer ds la RAM | |  |  | | --- | --- | |  |  | | **Adresses**  **16 bits** | **Contenu**  **8 bits** | |  | … | | 2A96 | M = T1\*T2 | |  | … | | 2B01 | 00000100 | | 2B02 | 11110100 | | 2B03 |  | |  |  |   Étape 7 : L’unité de contrôle demande à la RAM de placer le résultat à l’adresse 2B03 | variables |
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| |  |  |  | | --- | --- | --- | |  | Registres  (8 bits) |  | |  | M = T1\*T2 |  | |  | 00000100 | UAL | |  | 11110100 | |  | | --- | |  | | |  | 1101000 | |  |  | |  |  |  |  |  |  |  | | --- | --- | --- | |  |  |  | |  | Unité de contrôle |  | |  | |  |  | | --- | --- | |  |  | | **Adresses**  **16 bits** | **Contenu**  **8 bits** | |  | … | | 2A96 | M = T1\*T2 | |  | … | | 2B01 | 00000100 | | 2B02 | 11110100 | | 2B03 | 11010000 | |  |  |   Résultat : 11010000 (-48) dans la variable M (adresse 2B03) | variables |
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